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Appl. No. 10/743,985
Amdt. dated 07/05/2007
Response to Office Action of 04/05/2007

Attorney Docket No.: N1085-00168
[TSMC 2003-0219]

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1 1 - 10. (Cancelled)

1 11. (Currently Amended): An SOI device having a gate, comprising:
2 oxygen ions providing discrete implant regions in a substrate of an SOI device,
3 the discrete implant regions extending to a surface of the substrate;
4 one or more additional gate regions covering all discrete implant regions under
5 the one or more additional gate regions, and
6 a gate oxide layer covering but not encroaching the discrete implant regions and
7 being under the one or more additional gate regions,
8 the ~~ions~~ discrete implant regions forming gate oxide regions and reducing
9 substrate resistance under each of the additional gate regions.

1 12. (Original): The SOI device as recited in claim 11, further comprising:
2 implanted ions in the substrate, the one or more additional gate regions covering
3 the implanted ions.

1 13. (Previously Presented) The SOI device as recited in claim 11, wherein the gate
2 oxide layer has the same thickness over the discrete implant regions and over regions
3 other than the discrete implant regions.

1 14. (Previously Presented): The SOI device as recited in claim 11, further
2 comprising:
3 a gate of the SOI device.

1 15. (Previously Presented): The SOI device as recited in claim 11, further
2 comprising:

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3 a gate electrode layer forming an SOI device gate and the one or more additional
4 gate regions.

1 16. (Previously Presented): The SOI device as recited in claim 11, further
2 comprising:

3 an SOI device gate and the one or more additional gate regions being formed
4 from a gate electrode layer; and

5 wherein the gate oxide layer is under the gate and under the one or more
6 additional gate regions.

1 17. (Previously Presented): The SOI device as recited in claim 11, further
2 comprising:

3 the gate oxide layer including a thin gate oxide layer, and a thicker gate oxide
4 layer covering the discrete implant regions;

5 an SOI device gate on the thin gate oxide layer; and

6 the one or more additional gate regions being on the thicker gate oxide layer.

1 18. (Previously Presented): The SOI device as recited in claim 11, further
2 comprising:

3 the thicker gate oxide layer being a selective epitaxy growth.

1 19. (Currently Amended): The SOI device as recited in claim 11, further comprising:

2 the substrate having an STI enclosure for the ~~one~~ discrete implant regions.

1 20-35. (Cancelled)

1 36. (Currently Amended): An SOI device having a gate, comprising:

2 oxygen ions providing discrete implant regions in a substrate of an SOI device,

3 the discrete implant regions extending to a surface of the substrate;

4 one or more additional gate regions covering the discrete implant regions, and,

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5 a gate oxide layer formed over the surface and covering the discrete implant
6 regions and being under the one or more additional gate regions, the gate oxide layer
7 having the same thickness over the discrete implant regions and over regions other
8 than the discrete implant regions,

9 the ions discrete implant regions forming gate oxide regions and reducing
10 substrate resistance under each of the additional gate regions.

1 37. (New): The SOI device of claim 11, further comprising doped ion implants under
2 at least one of the one or more additional gate regions, the doped ion implants forming
3 a source and drain in the substrate.

1 38. (New): The SOI device of claim 37 wherein the substrate is a P-substrate, and
2 the doped ion implants are N+ doped ions.

1 39. (New): The SOI device of claim 37 wherein the substrate is an N-substrate, and
2 the doped ion implants are P+ doped ions.

1 40. (New): The SOI device of claim 36, further comprising doped ion implants under
2 at least one of the one or more additional gate regions, the doped ion implants forming
3 a source and drain in the substrate.

1 41. (New): An SOI device having a gate, comprising:
2 a plurality of gate regions covering thick oxide regions and thin oxide regions,
3 each said thick oxide region comprising a discrete implant region of oxygen ions
4 formed in a substrate of an SOI device and extending to a surface of the substrate, and
5 an oxide layer formed over but not encroaching the surface; and
6 each said thin oxide region comprising only said oxide layer,
7 said oxide layer having substantially the same thickness in said thick oxide
8 regions and said thin oxide regions.

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- 1 42. (New): The SOI device of claim 41, further comprising doped ion implants under at least one of the plurality of gate regions, the doped ion implants forming a source and drain in the substrate.
- 1 43. (New): The SOI device of claim 42 wherein the substrate is a P-substrate, and the doped ion implants are N+ doped ions.
- 1 44. (New): The SOI device of claim 42 wherein the substrate is an N-substrate, and the doped ion implants are P+ doped ions.
- 1 45. (New): The SOI device of claim 42 wherein each of the plurality of gate regions is formed of polysilicon and includes sidewall spacers on opposed sidewalls thereof.
- 1 46. (New): The SOI device of claim 41 wherein each of the plurality of gate regions is formed of polysilicon.